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UNIFIED MATRICES FOR ELECTRONIC COMPUTERS(U) FOREIGN
TECHNOLOGY DIV WRIGHT-PATTERSON AFB OH 27 JAN 86
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FOREIGN TECHNOLOGY DIVISION



UNIFIED MATRICES FOR ELECTRONIC COMPUTERS



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EDITED TRANSLATION

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UNIFIED MATRICES FOR ELECTRONIC COMPUTERS

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WP.AFB, OHIO.

U. S. BOARD ON GEOGRAPHIC NAMES TRANSLITERATION SYSTEM

Block	Italic	Transliteration	Block	Italic	Transliteration
А а	<i>А а</i>	A, a	Р р	<i>Р р</i>	R, r
Б б	<i>Б б</i>	B, b	С с	<i>С с</i>	S, s
В в	<i>В в</i>	V, v	Т т	<i>Т т</i>	T, t
Г г	<i>Г г</i>	G, g	У у	<i>У у</i>	U, u
Д д	<i>Д д</i>	D, d	Ф ф	<i>Ф ф</i>	F, f
Е е	<i>Е е</i>	Ye, ye; E, e*	Х х	<i>Х х</i>	Kh, kh
Ж ж	<i>Ж ж</i>	Zh, zh	Ц ц	<i>Ц ц</i>	Ts, ts
З з	<i>З з</i>	Z, z	Ч ч	<i>Ч ч</i>	Ch, ch
И и	<i>И и</i>	I, i	Ш ш	<i>Ш ш</i>	Sh, sh
Й й	<i>Й й</i>	Y, y	Щ щ	<i>Щ щ</i>	Shch, shch
К к	<i>К к</i>	K, k	Ъ ъ	<i>Ъ ъ</i>	"
Л л	<i>Л л</i>	L, l	Ы ы	<i>Ы ы</i>	Y, y
М м	<i>М м</i>	M, m	Ь ь	<i>Ь ь</i>	'
Н н	<i>Н н</i>	N, n	Э э	<i>Э э</i>	E, e
О о	<i>О о</i>	O, o	Ю ю	<i>Ю ю</i>	Yu, yu
П п	<i>П п</i>	P, p	Я я	<i>Я я</i>	Ya, ya

*ye initially, after vowels, and after ъ, ь; e elsewhere.
When written as ë in Russian, transliterate as yë or ë.

RUSSIAN AND ENGLISH TRIGONOMETRIC FUNCTIONS

Russian	English	Russian	English	Russian	English
sin	sin	sh	sinh	arc sh	sinh ⁻¹
cos	cos	ch	cosh	arc ch	cosh ⁻¹
tg	tan	th	tanh	arc th	tanh ⁻¹
ctg	cot	cth	coth	arc cth	coth ⁻¹
sec	sec	sch	sech	arc sch	sech ⁻¹
cosec	csc	csch	csch	arc csch	csch ⁻¹

Russian English

rot curl
lg log

GRAPHICS DISCLAIMER

All figures, graphics, tables, equations, etc. merged into this translation were extracted from the best quality copy available.

UNIFIED MATRICES FOR
ELECTRONIC COMPUTERS
Main Parameters

GOST
14288-69

By the Decree of the Committee of Standards, Measures, and Measuring Instruments, USSR Council of Ministers, from 3/6/1969, No. 330, in Effect since 1/1/1970

Violation of the Standard is Prosecuted in Accordance
with the Law

1. This standard extends to the ferrite-core matrices operating on the 2D principle, which are intended for the storage units of the general-purpose electronic computers using the number system with a base of 2.

2. Matrices must be manufactured with a capacity of 256, 1024, 4096, (8192), 16384, (32768), 65536 of binary storage elements.

The matrix capacities in parentheses are not to be used in the new designs of storage units.

3. The construction of frames must ensure the following space between the coordinate leads: 2.0, 1.5, 1.2, 1.0, 0.8, 0.6, 0.4, and 0.2 mm.

4. The following parameters must be shown in the matrix's technical documentation:

- a) static: ohmic resistance and inductance of windings;
- b) dynamic: parameters of input currents; operating cycle of matrices; magnitude of amplitude and duration of signals of counted units and interferences obtained from matrices during a change in the operating recording currents (inhibition) and coordinate access currents; magnitude of amplitude and duration of interferences in the read and record windings during unfavorable operating conditions of a computer.

5. Mechanical, climatic, and reliability requirements, and also special requirements must be shown in the technical documentation of a

matrix.

6. The matrices must be identified by an alphanumeric code, which includes:

- storage core control principle;
- space between the coordinate leads;
- type of unified frame used in the matrix;
- type and external diameter of a core separated from one another by separating points.

An example of designating a matrix operating on the ZD principle with a step of 1.5 between the coordinate leads, a unified frame of type M2-2, and an external diameter of a circular storage core of 0.8:

Matrix 3D.1.5. M2-2. K-0.8 GOST 14288-69

Supplement to GOST 14288-69

Definition of Basic Terms Encountered in the Standard

Matrix - a set of ferrite storage cores structurally unified in the same frame by a system of wires.

ZD Principle - a method of controlling a storage core, in which changing a core from one state to another is accomplished by the effect of an algebraic sum of two, during reading, and three, during recording, partial currents; in this case, each partial current is equal to a half of the total switching current.

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